

SUPPLEMENTAL PRELIMINARY AMENDMENT

Page 2

Serial Number: 09/484,303

Filing Date: January 18, 2000

Title: METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALSIN THE CLAIMS

- 1-4. (Previously Canceled)
5. (Original) A method comprising:
forming a conductive structure;
forming a diffusion-barrier lining around the conductive structure after forming the conductive structure; and
forming an insulative structure around the conductive structure after forming the diffusion-barrier lining.
6. (Original) The method of claim 5, wherein forming the conductive structures comprises applying a copper-, silver-, or gold-based material.
7. (Original) The method of claim 5, wherein forming the conductive structure comprises:
ionized sputtering or DC magnetron sputtering of a copper-based material onto at least a portion of the diffusion barrier; and
electroplating a copper-based material onto the sputtered copper-based material.
8. (Original) The method of claim 5, wherein forming the insulative structure comprises spin-coating an aerogel or xerogel.
9. (Original) The method of claim 5, wherein forming the diffusion-barrier lining comprises forming a graded composition of WSi_x , where x varies from 2.0 to 2.5.
10. (Original) The method of claim 5, wherein forming the diffusion-barrier lining comprises:
forming a graded composition of WSi_x , where x varies from 2.0 to 2.5; and
nitriding the graded composition of WSi_x .

SUPPLEMENTAL PRELIMINARY AMENDMENT

Page 3

Serial Number: 09/484,303

Filing Date: January 18, 2000

Title: METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS

11. (Original) The method of claim 5 wherein nitriding the graded composition of WSi₆ comprises exciting a plasma with argon gas.

12. (Original) The method of claim 5, wherein forming the diffusion-barrier lining comprises:

introducing tungsten hexafluoride and hydrogen gases into a wafer processing chamber for a predetermined amount of time;

introducing silane gas into the chamber a first predetermined time after introducing the tungsten hexafluoride gas; and

terminating introduction of the silane gas a second predetermined time before terminating introduction of the tungsten hexafluoride and hydrogen gases into the chamber.

13. (Original) The method of claim 5, wherein the first and second times are in the range of about one to about three seconds.

14-35. (Previously Canceled)

36. (Withdrawn) A method of making an integrated memory circuit, comprising:

forming a first mask layer having one or more openings or trenches, with each opening exposing a portion of one or more transistor contact regions;

forming a first gold-based conductive structure on the first mask layer, with the first gold-based conductive structure having one or more portions contacting at least one of the exposed transistors contact regions;

forming a second mask layer having one or more openings or trenches, with each opening exposing a portion of the first conductive structure;

forming a second gold-based conductive structure on the second mask layer, with one or more portions of the second gold-based conductive structure contacting at least one of the exposed portions of the first gold-based conductive structure;

removing in a single procedure at least respective portions of the first and second mask structures after forming the second gold-based conductive structure;

SUPPLEMENTAL PRELIMINARY AMENDMENT

Page 4

Serial Number: 09/484.303

Filing Date: January 18, 2000

Title: METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS

forming in a single procedure a diffusion barrier on at least respective portions of the first and second gold-based conductive structures after removing at least the respective portions of the first and second mask structures; and

forming in a single procedure an insulator on and between the first and second gold-based conductive structures after forming the diffusion barrier.

37. (Withdrawn) The method of claim 36:

wherein forming the first and second mask layers comprises depositing photoresist;

wherein removing the first and second mask layers comprises ashing the first and second mask layers; and

wherein forming the insulator on and between the first and second conductive structures comprises spin-coating the first and second gold-based conductive structures with an aerogel or xerogel.

38. (Withdrawn) A method of making an integrated memory circuit, comprising:

forming a first mask layer having one or more openings or trenches, with each opening exposing a portion of one or more transistor contact regions;

forming a first silver-based conductive structure on the first mask layer, with the first silver-based conductive structure having one or more portions contacting at least one of the exposed transistors contact regions;

forming a second mask layer having one or more openings or trenches, with each opening exposing a portion of the first conductive structure;

forming a second silver-based conductive structure on the second mask layer, with one or more portions of the second silver-based conductive structure contacting at least one of the exposed portions of the first silver-based conductive structure;

removing in a single procedure at least respective portions of the first and second mask structures after forming the second silver-based conductive structure;

forming in a single procedure a diffusion barrier on at least respective portions of the first and second silver-based conductive structures after removing at least the respective portions of the first and second mask structures; and

SUPPLEMENTAL PRELIMINARY AMENDMENT

Page 5

Serial Number: 09/484,303

Filing Date: January 18, 2000

Title: METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS

forming in a single procedure an insulator on and between the first and second silver-based conductive structures after forming the diffusion barrier.

39. (Withdrawn) The method of claim 38:

wherein forming the first and second mask layers comprises depositing photoresist;

wherein removing the first and second mask layers comprises ashing the first and second mask layers; and

wherein forming the insulator on and between the first and second conductive structures comprises spin-coating the first and second silver-based conductive structures with an aerogel or xerogel.

40. (Withdrawn) A method of making an integrated memory circuit, comprising:

forming a first mask layer having one or more openings or trenches, with each opening exposing a portion of one or more transistor contact regions;

forming a first copper-based conductive structure on the first mask layer, with the first copper-based conductive structure having one or more portions contacting at least one of the exposed transistors contact regions;

forming a second mask layer having one or more openings or trenches, with each opening exposing a portion of the first conductive structure;

forming a second copper-based conductive structure on the second mask layer, with one or more portions of the second copper-based conductive structure contacting at least one of the exposed portions of the first copper-based conductive structure;

removing in a single procedure at least respective portions of the first and second mask structures after forming the second copper-based conductive structure;

forming in a single procedure a diffusion barrier on at least respective portions of the first and second copper-based conductive structures after removing at least the respective portions of the first and second mask structures; and

forming in a single procedure an insulator on and between the first and second copper-based conductive structures after forming the diffusion barrier.

SUPPLEMENTAL PRELIMINARY AMENDMENT

Page 6

Serial Number: 09/484,303

Filing Date: January 18, 2000

Title: METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS

41. (Withdrawn) The method of claim 40:

wherein forming the first and second mask layers comprises depositing photoresist;

wherein removing the first and second mask layers comprises ashing the first and second mask layers; and

wherein forming the insulator on and between the first and second conductive structures comprises spin-coating the first and second copper-based conductive structures with an aerogel or xerogel.

42. (Previously Canceled)

43. (New) A method comprising:

forming a first conductive structure with contact plugs that contact an integrated circuit substrate, and wired portions that intersect at least some of the contact plugs;

forming a diffusion-barrier lining on exposed portions of the first conductive structure after forming the first conductive structure; and

forming an insulative structure in spaces around and between portions of the first conductive structure after forming the diffusion-barrier lining.

44. (New) The method of claim 43, wherein forming the first conductive structure comprises:

forming a mask layer on the substrate with contact plug holes that open to the integrated circuit substrate, and trenches intersecting at least some of the contact plug holes;

depositing a seed layer over the mask layer;

electroplating conductive material over the seed layer to form the contact plugs;

removing excess material to form the wired portions; and

removing at least a portion of the mask layer to form the spaces between the portions of the first conductive structure.

SUPPLEMENTAL PRELIMINARY AMENDMENT

Page 7

Serial Number: 09/484,303

Filing Date: January 18, 2000

Title: METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS

45. (New) The method of claim 44, further comprising:

forming a second conductive structure on top of the first conductive structure before removing the portion of the mask layer.

46. (New) The method of claim 44, further comprising:

forming an adhesion layer over the mask layer before electroplating.

47. (New) A method comprising:

forming a conductive structure from a material that includes copper, wherein the conductive structure includes contact plugs that contact an integrated circuit substrate, and wired portions that intersect at least some of the contact plugs;

forming a diffusion-barrier lining on exposed portions of the conductive structure after forming the conductive structure; and

forming an insulative structure in spaces around and between portions of the conductive structure after forming the diffusion-barrier lining.

48. (New) The method of claim 47, wherein forming the diffusion-barrier lining comprises:

forming a layer of tungsten silicon nitrogen over substantially all of the exposed portions of the conductive structure.

49. (New) The method of claim 47, wherein forming the diffusion-barrier lining comprises:

forming a layer of tungsten silicide over substantially all of the exposed portions of the conductive structure, and

nitriding the layer of tungsten silicide to form a layer of tungsten silicon nitrogen.

50. (New) A method comprising:

forming a conductive structure with contact plugs that contact an integrated circuit substrate, and wired portions that intersect at least some of the contact plugs;

forming a diffusion-barrier lining on substantially all exposed portions of the conductive structure after forming the conductive structure by forming a layer of tungsten silicon nitrogen over substantially all of the exposed portions of the conductive structure; and

SUPPLEMENTAL PRELIMINARY AMENDMENT

Page 8

Serial Number: 09/484,303

Filing Date: January 18, 2000

Title: METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS

forming an insulative structure in spaces around and between portions of the conductive structure after forming the diffusion-barrier lining.

51. (New) The method of claim 50, wherein forming the diffusion-barrier lining comprises:
forming the diffusion-barrier lining with a thickness in a range of two to ten nanometers over substantially all of the exposed portions of the conductive structure.

52. (New) A method comprising:
forming a conductive structure with contact plugs that contact an integrated circuit substrate, and wired portions that intersect at least some of the contact plugs;
forming a diffusion-barrier lining on substantially all exposed portions of the conductive structure after forming the conductive structure by forming a layer of tungsten silicide over substantially all of the exposed portions of the conductive structure; and
nitriding the layer of tungsten silicide to form a layer of tungsten silicon nitrogen; and
forming an insulative structure in spaces around and between portions of the conductive structure after forming the diffusion-barrier lining.

53. (New) The method of claim 52, wherein forming the diffusion-barrier lining comprises:
forming the diffusion-barrier lining with a thickness in a range of two to ten nanometers over substantially all of the exposed portions of the conductive structure.

54. (New) A method comprising:
forming a conductive structure with contact plugs that contact an integrated circuit substrate, and wired portions that intersect at least some of the contact plugs;
forming a diffusion-barrier lining on substantially all exposed portions of the conductive structure after forming the conductive structure, wherein the diffusion-barrier lining has a thickness in a range of two to ten nanometers over substantially all of the exposed portions of the conductive structure; and
forming an insulative structure in spaces around and between portions of the conductive structure after forming the diffusion-barrier lining.

SUPPLEMENTAL PRELIMINARY AMENDMENT

Page 9

Serial Number: 09/484,303

Filing Date: January 18, 2000

Title: METHODS FOR MAKING INTEGRATED-CIRCUIT WIRING FROM COPPER, SILVER, GOLD, AND OTHER METALS

55. (New) The method of claim 54, wherein forming the diffusion-barrier lining comprises:
forming a layer of tungsten silicon nitrogen over substantially all of the exposed portions
of the conductive structure.
56. (New) The method of claim 54, wherein forming the diffusion-barrier lining comprises:
forming a layer of tungsten silicide over substantially all of the exposed portions of the
conductive structure; and
nitriding the layer of tungsten silicide to form a layer of tungsten silicon nitrogen.
57. (New) A method comprising:
forming a conductive structure with contact plugs that contact an integrated circuit
substrate, and wired portions that intersect at least some of the contact plugs;
forming a diffusion-barrier lining on exposed portions of the conductive structure after
forming the conductive structure; and
forming an insulative structure in spaces around and between portions of the conductive
structure after forming the diffusion-barrier lining, wherein the insulative structure is formed by
depositing a material that includes silicon oxide in the spaces.
58. (New) The method of claim 57, wherein forming the diffusion-barrier lining comprises:
forming a layer of tungsten silicon nitrogen over substantially all of the exposed portions
of the conductive structure.
59. (New) The method of claim 57, wherein forming the diffusion-barrier lining comprises:
forming a layer of tungsten silicide over substantially all of the exposed portions of the
conductive structure; and
nitriding the layer of tungsten silicide to form a layer of tungsten silicon nitrogen.
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